FIG.1A

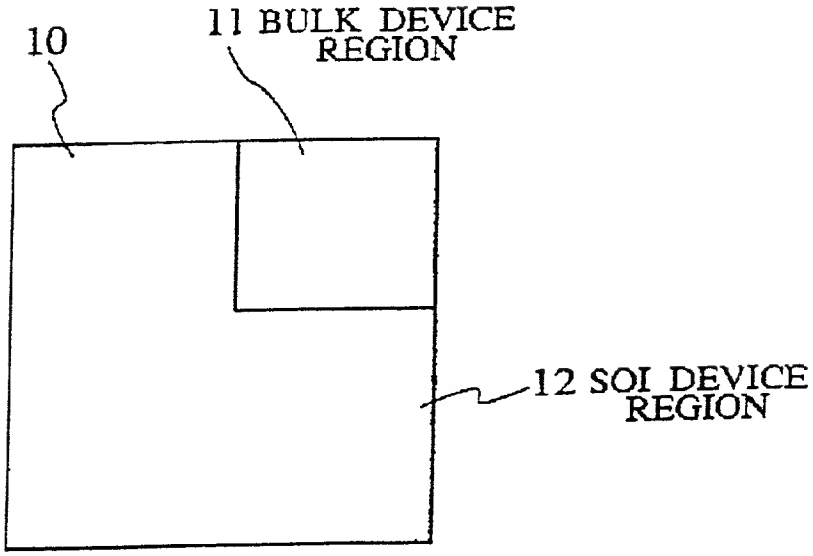

FIG.1B

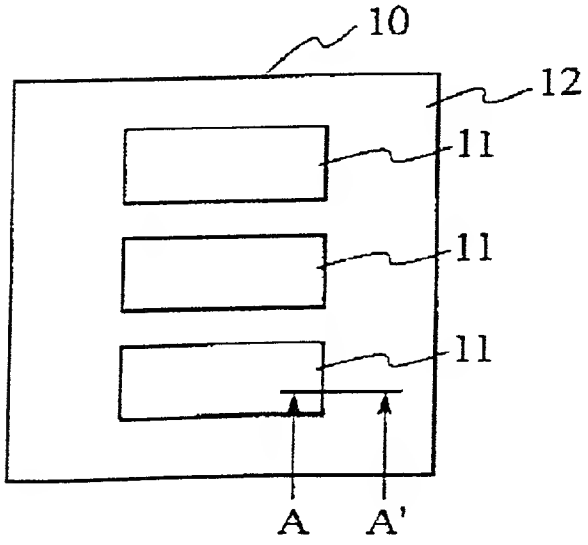

FIG.2

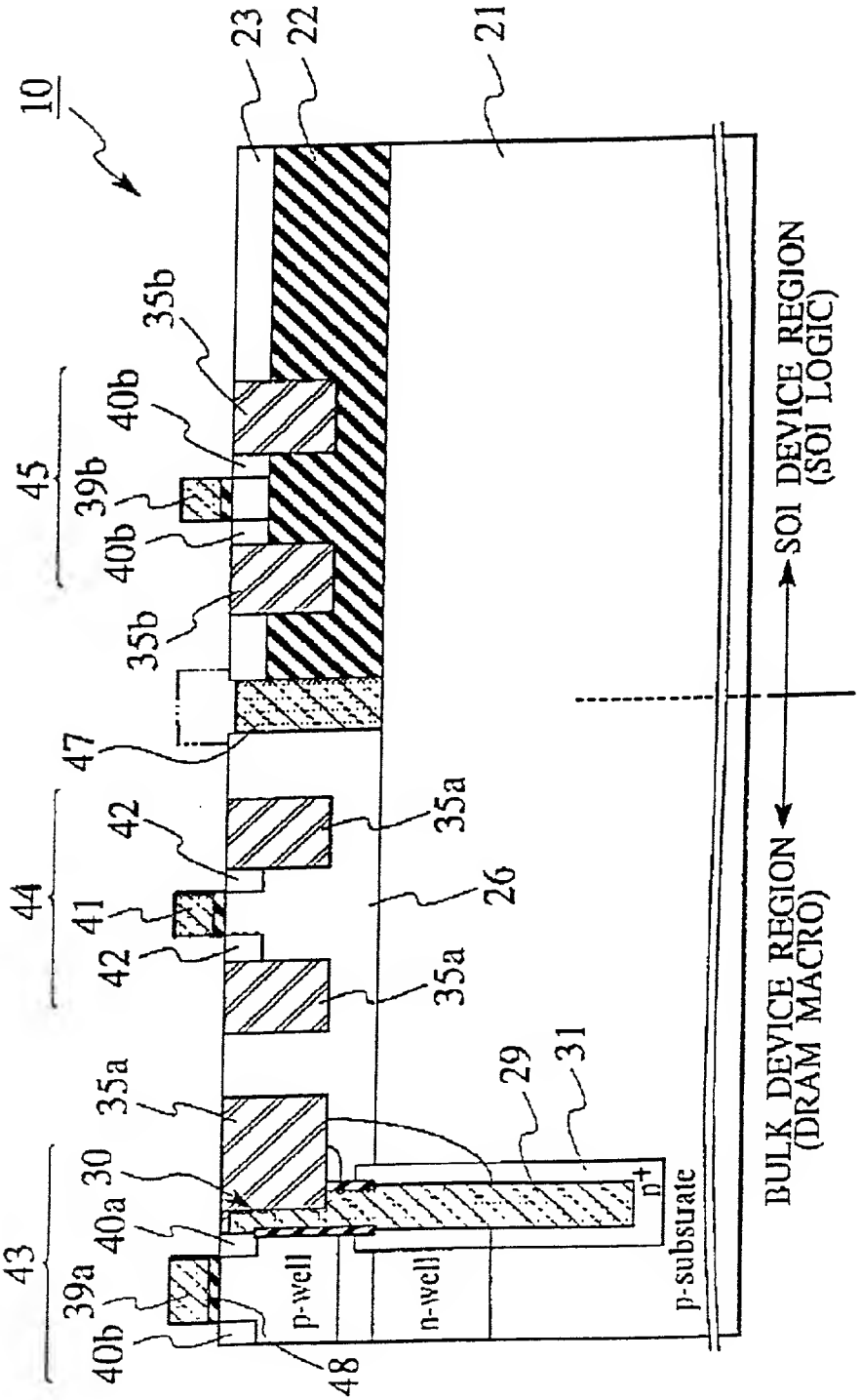
10
23
22
21
35b
40b
45
39b
40b
35b
47
42
35a
44
41
42
26
35a
35a
29
31
30
40a
43
39a
40b
48
p-well
n-well
n+
p-substrate
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.3A

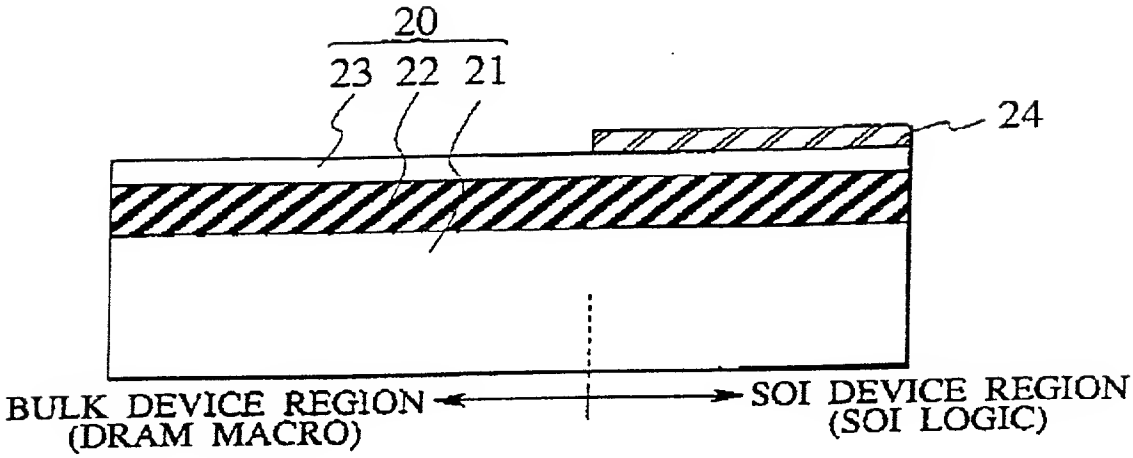

FIG.3B

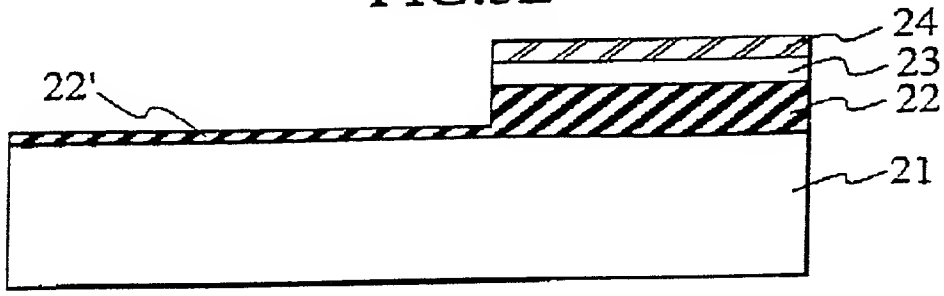

FIG.3C

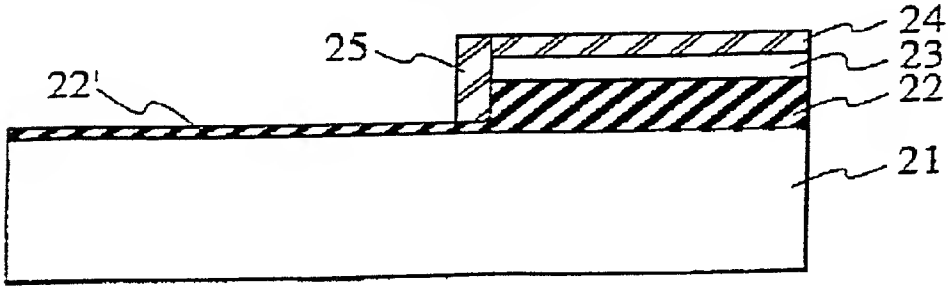

FIG.3D

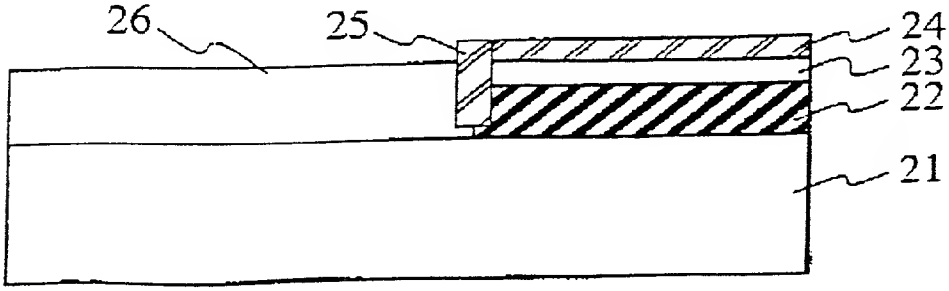

FIG.3E

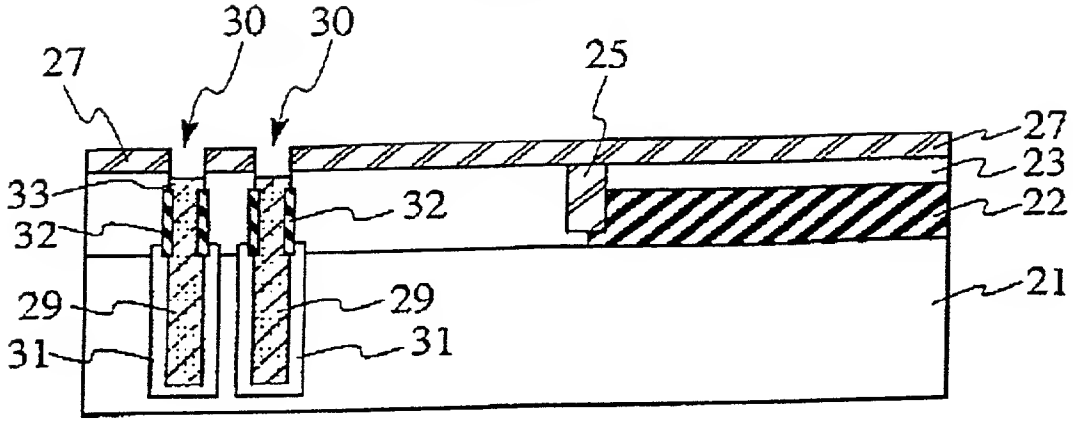

FIG.3F

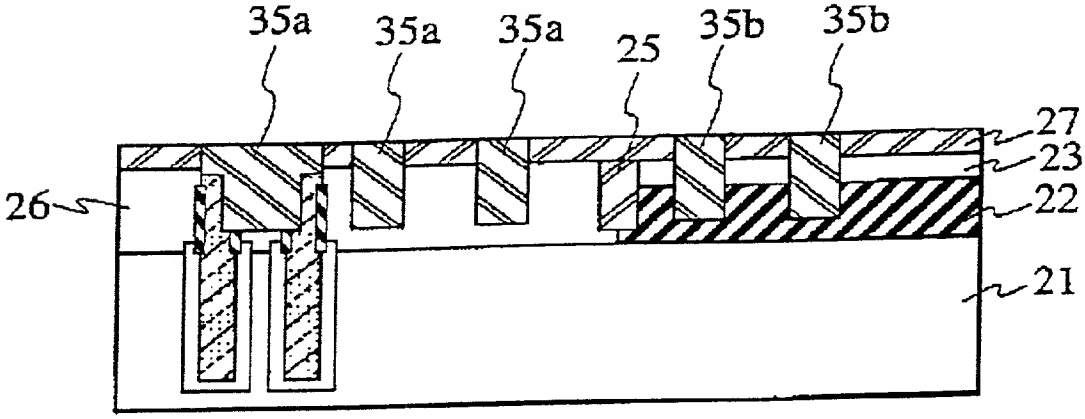

FIG.3G

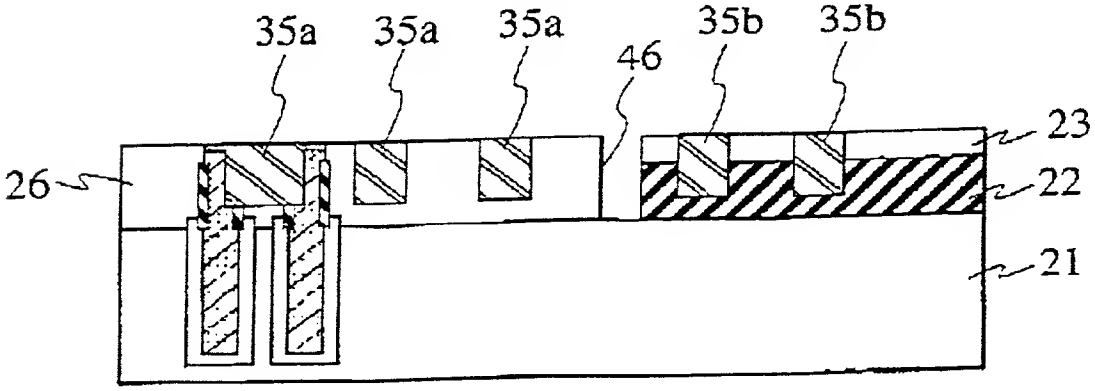

FIG.4

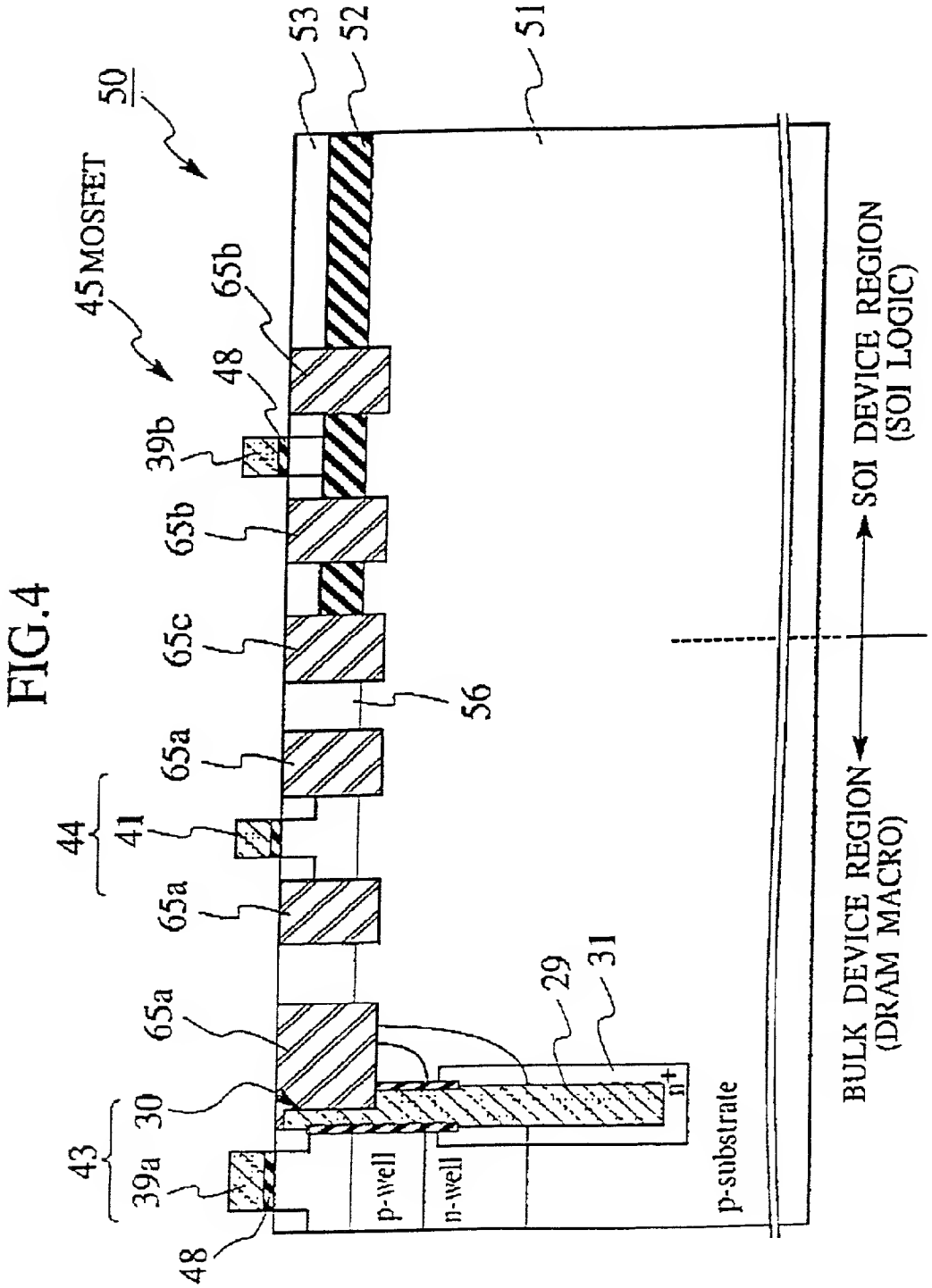
50
45 MOSFET
53
52
51
65b
48
39b
65b
65c
56
65a
44
41
65a
65a
29
31
30
43
39a
48
p-well
n-well
n+
p-substrate
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.5A

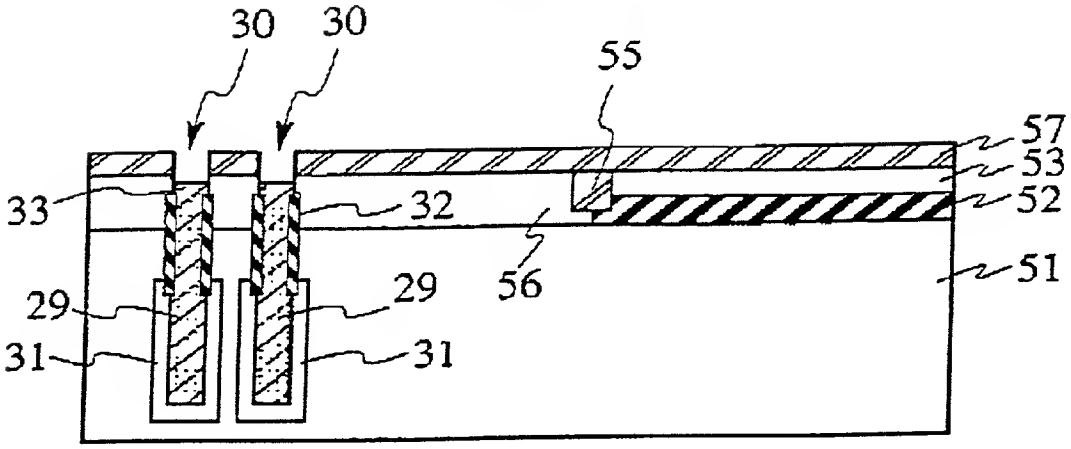

FIG.5B

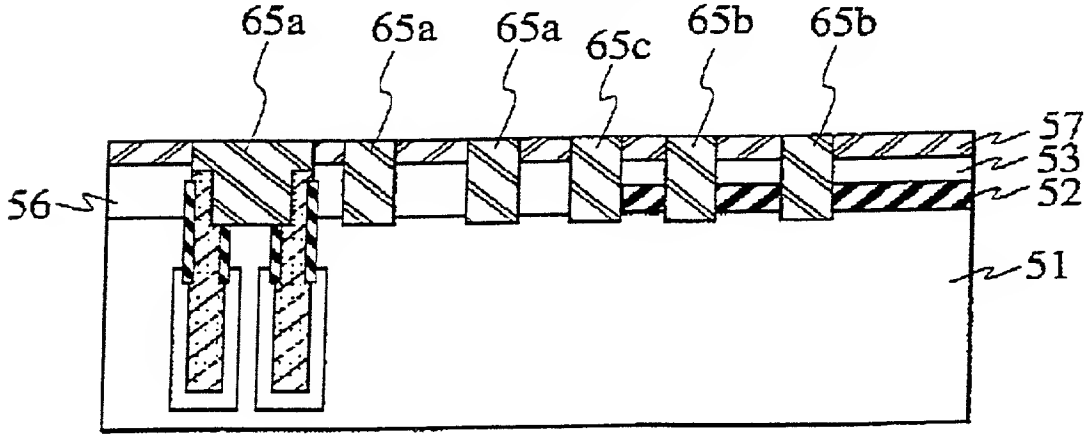

FIG.5C

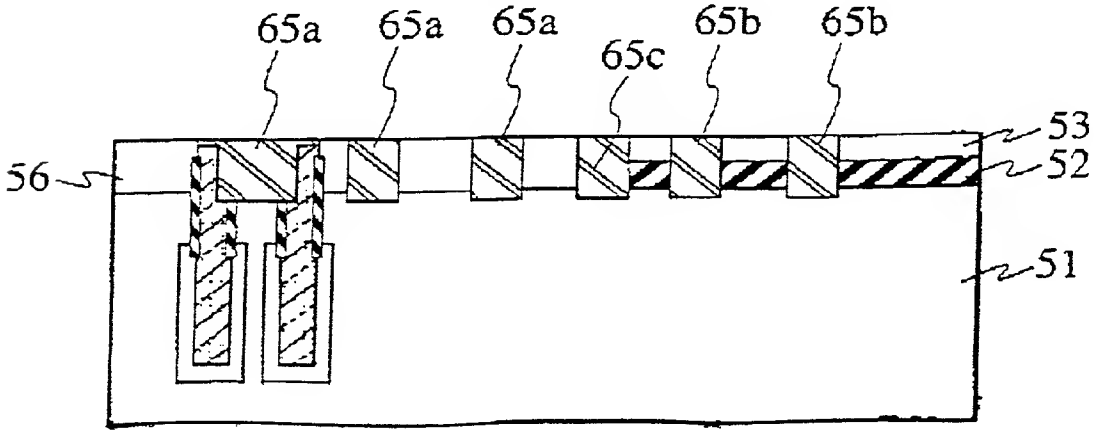

FIG.6

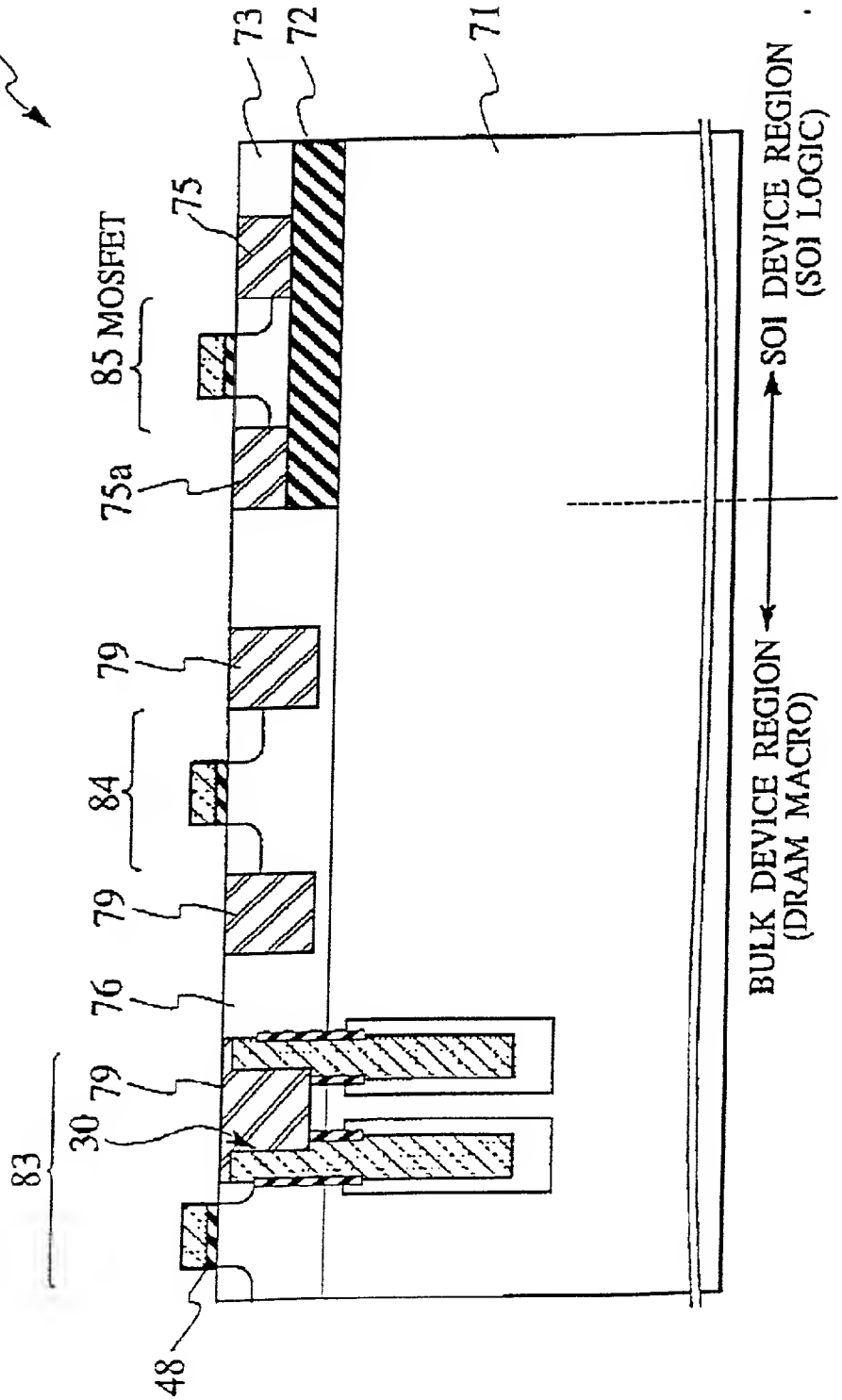
70
73
72
71
75
85 MOSFET
75a
79
84
79
76
79
30
83
48
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.7A

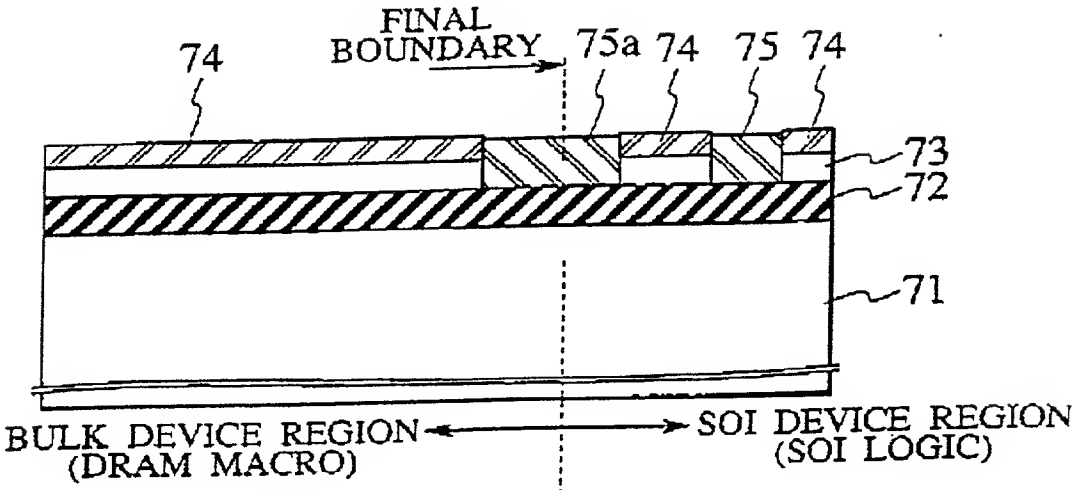

FIG.7B

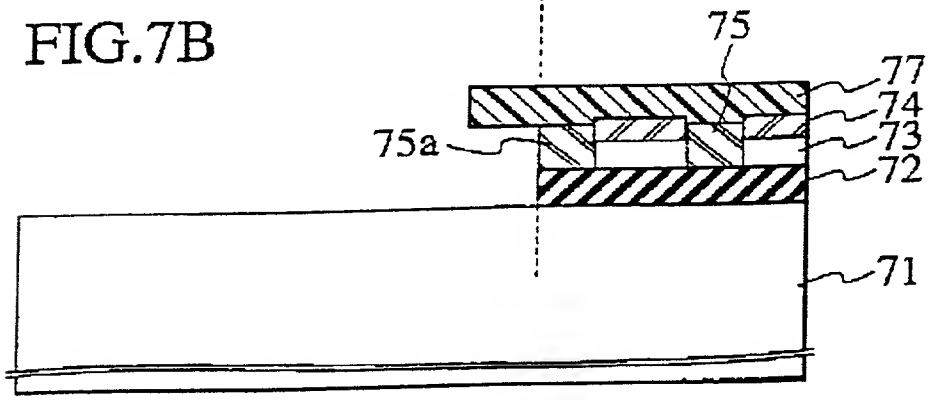

FIG.7C

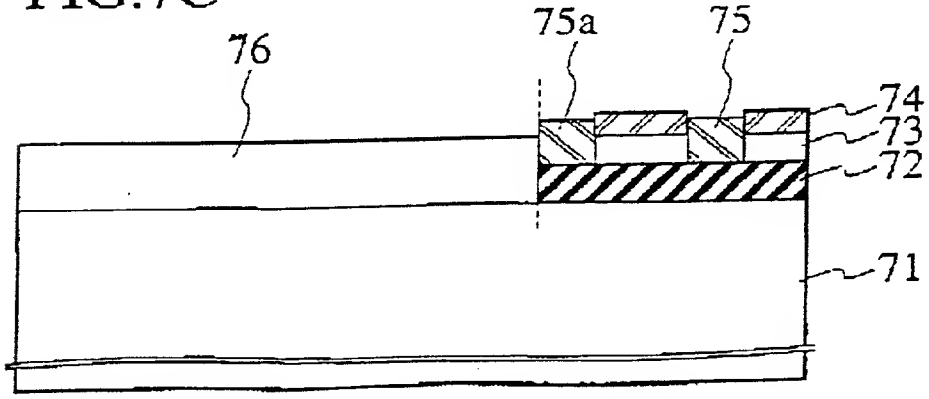

FIG.7D

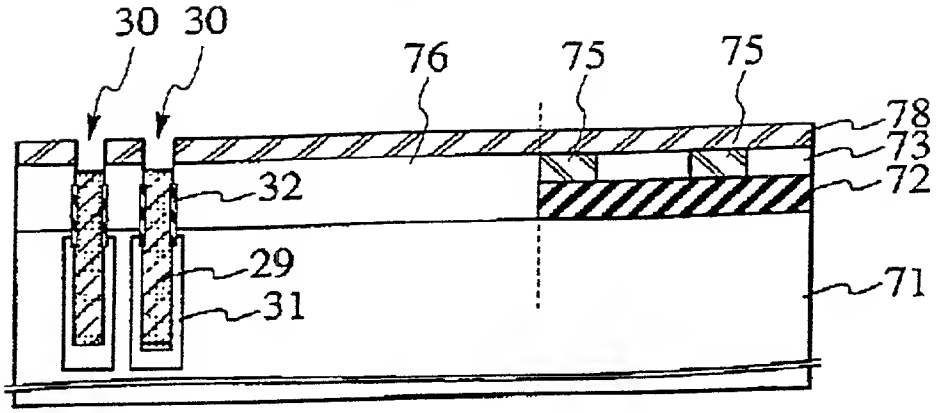

FIG.7E

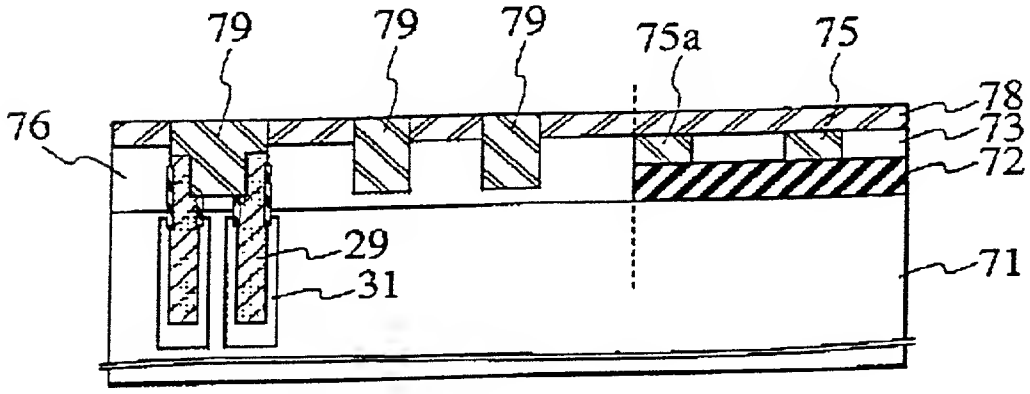

FIG.7F

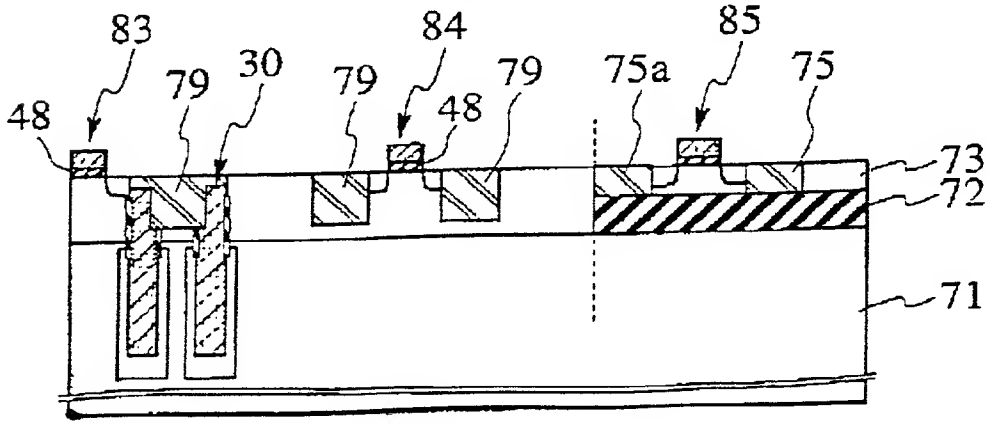

FIG.8A

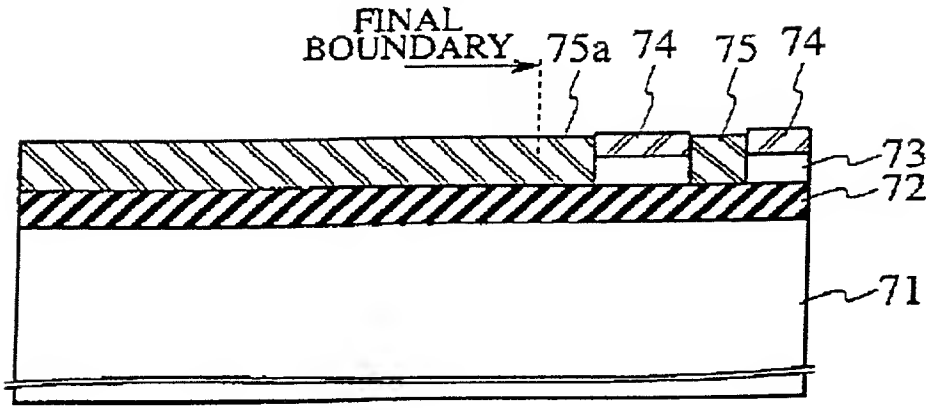

FIG.8B

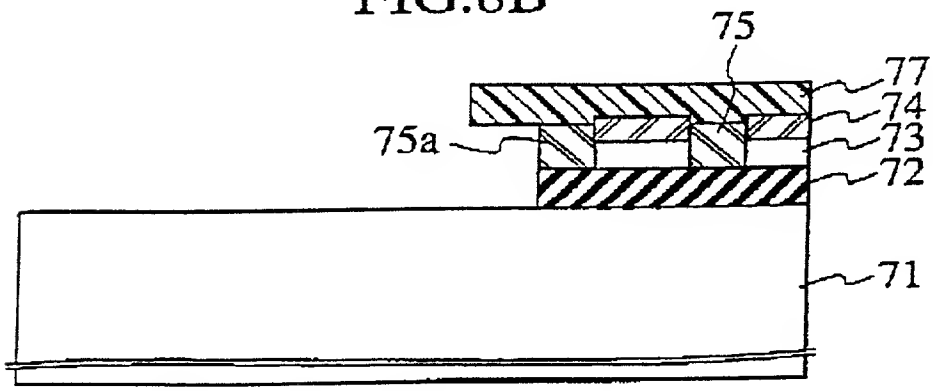

FIG.8C

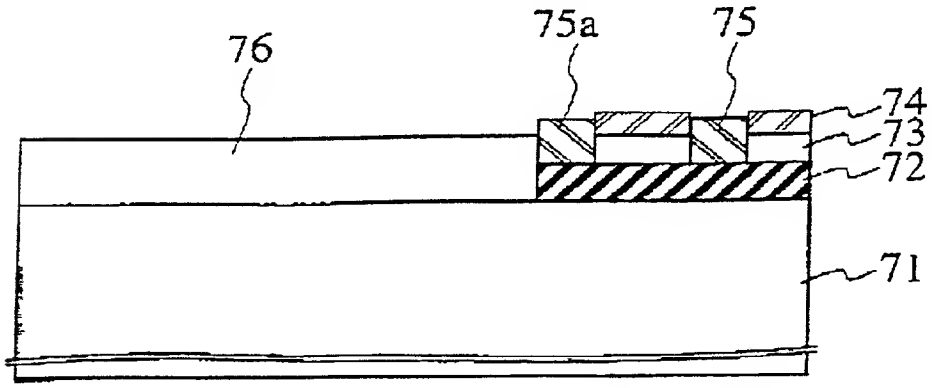

FIG.9A

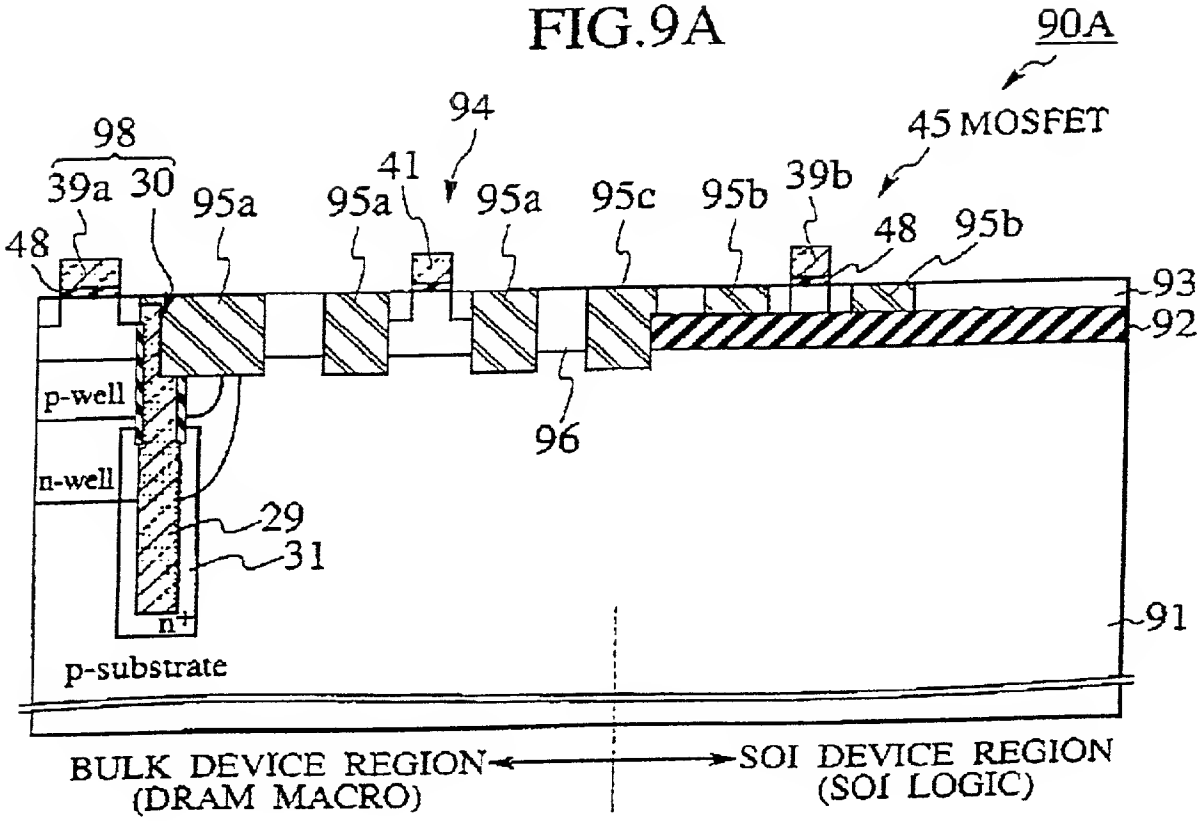
90A
45 MOSFET
98
39a 30
95a
94
41
95a
95a
95c
95b
39b
48
95b
48
93
92
p-well
n-well
96
29
31
n+
91
p-substrate
BULK DEVICE REGION
(DRAM MACRO)
SOI DEVICE REGION
(SOI LOGIC)

FIG.9B

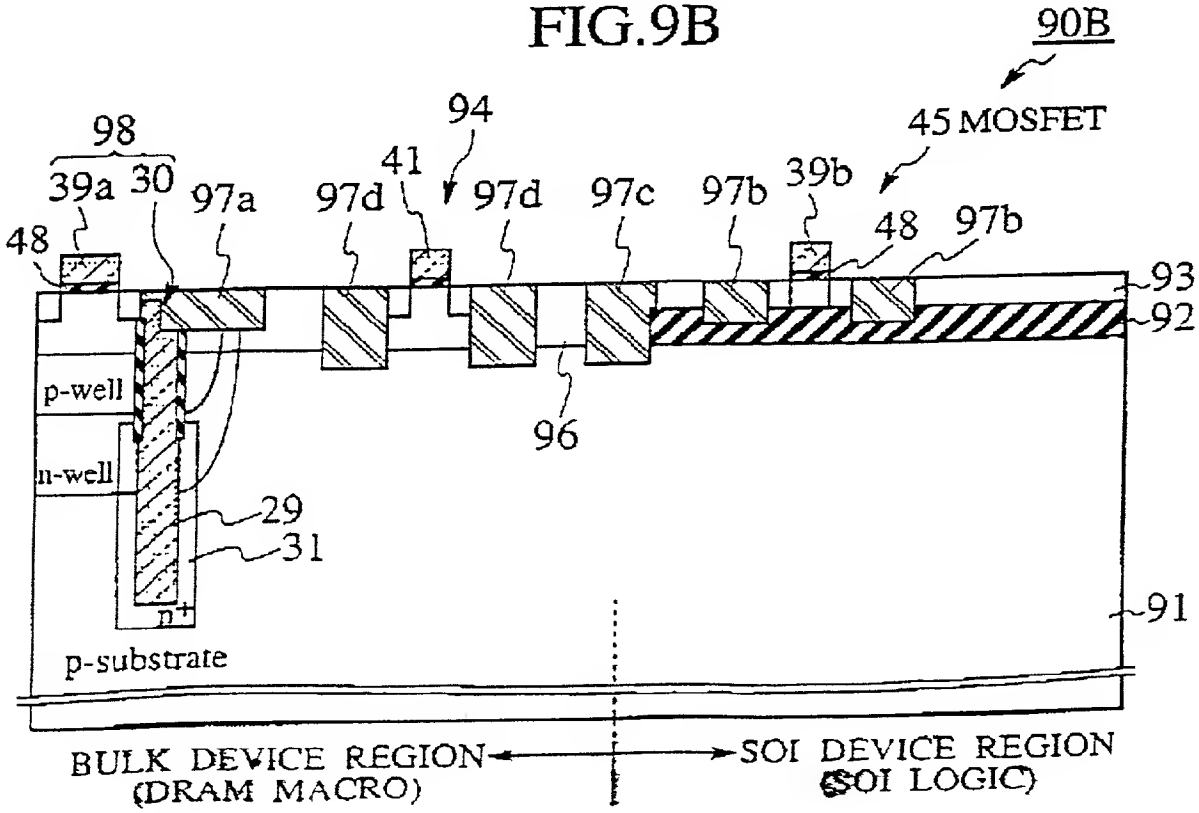
90B
45 MOSFET
98
39a 30
97a
94
41
97d
97d
97c
97b
39b
48
97b
48
93
92
p-well
n-well
96
29
31
n+
91
p-substrate
BULK DEVICE REGION
(DRAM MACRO)
SOI DEVICE REGION
(SOI LOGIC)

FIG.10

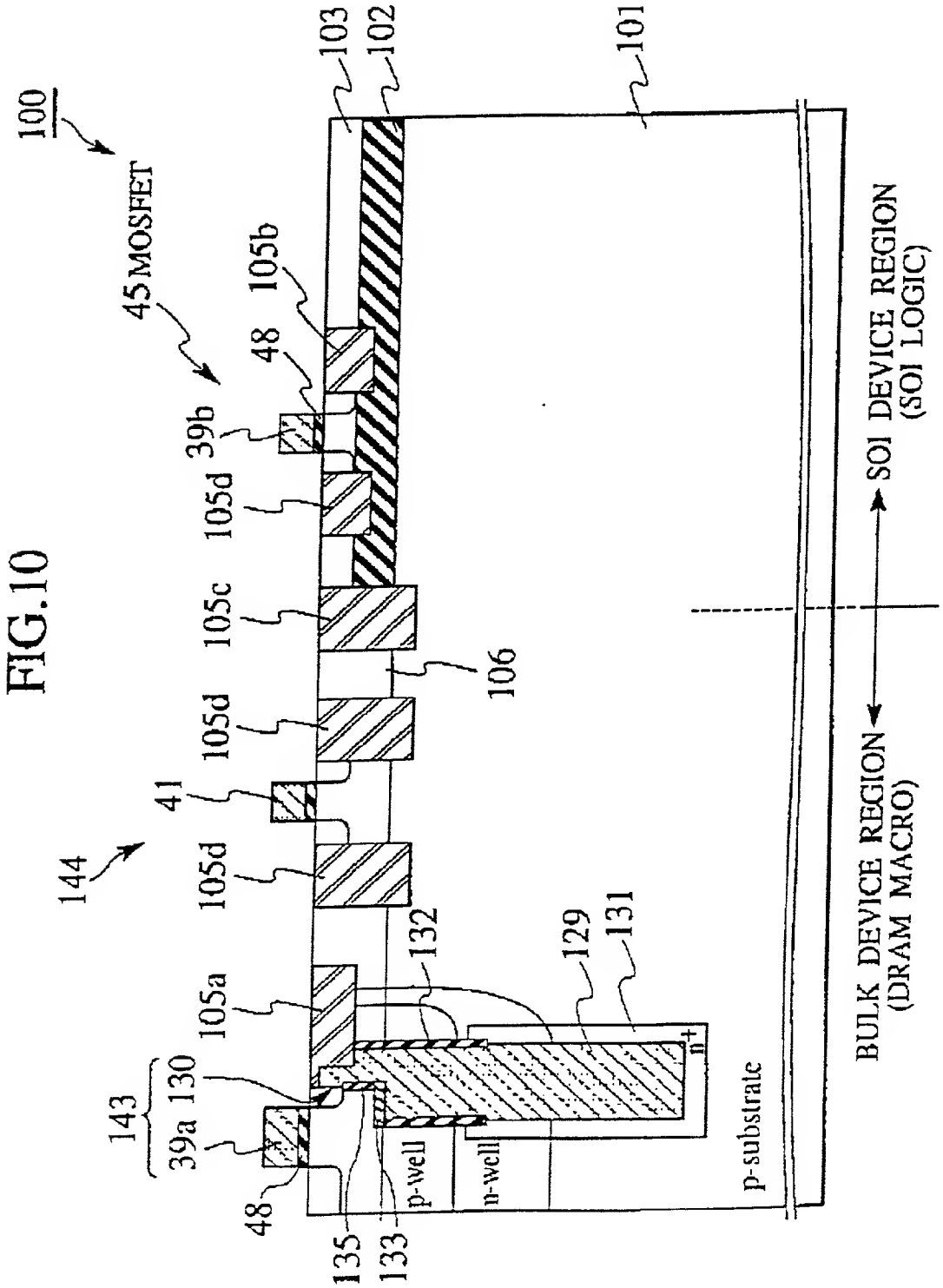
100
45 MOSFET
103
102
101
105b
48
39b
105d
105c
106
105d
41
105d
144
105a
132
129
131
143
39a 130
48
135
133
p-well
n-well
n+
p-substrate
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.11A

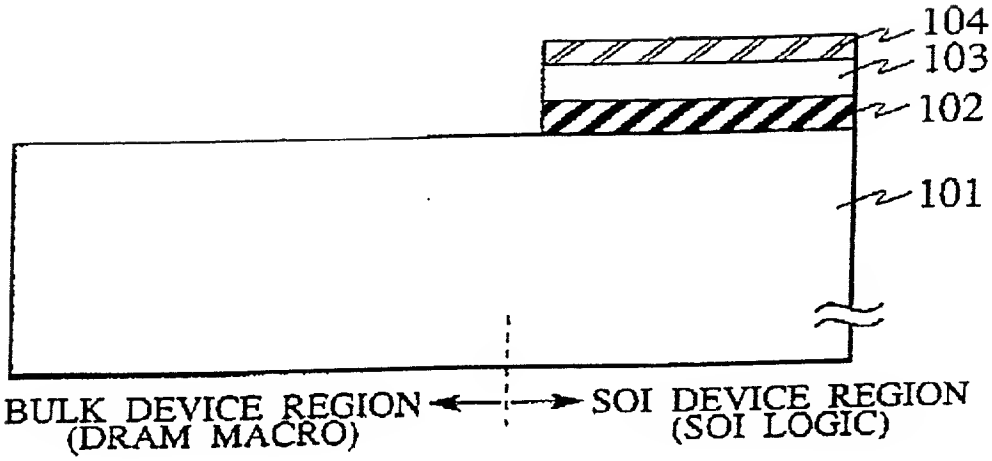

FIG.11B

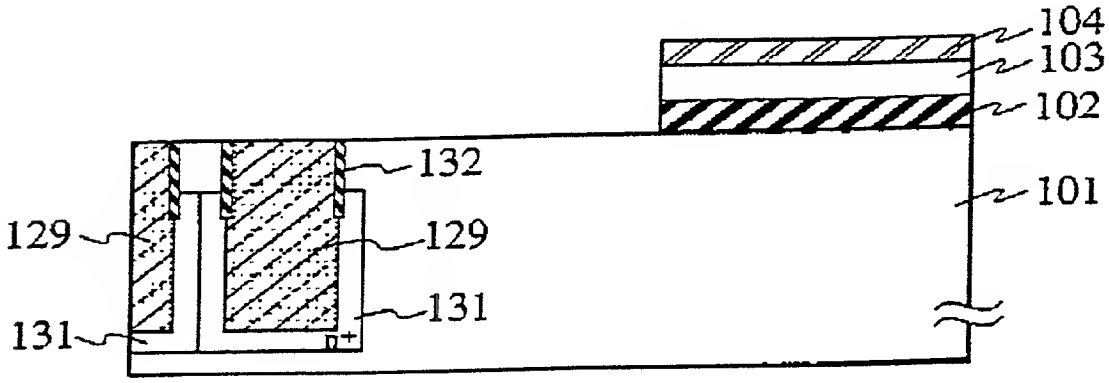

FIG.11C

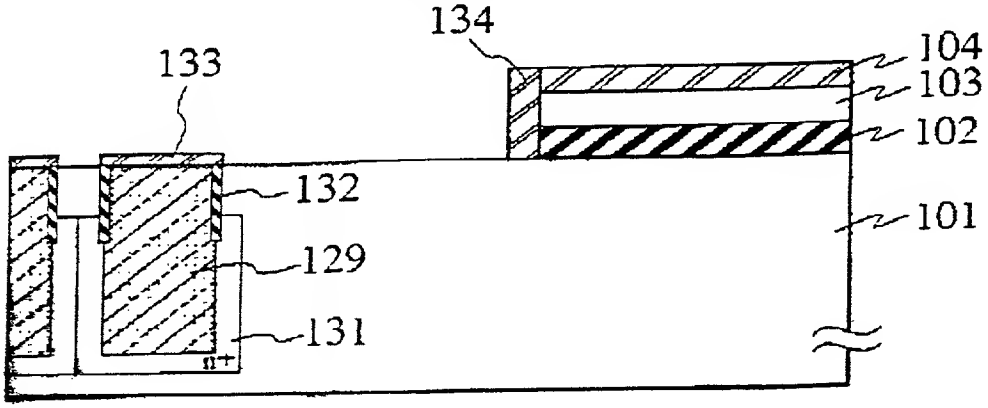

FIG.11D

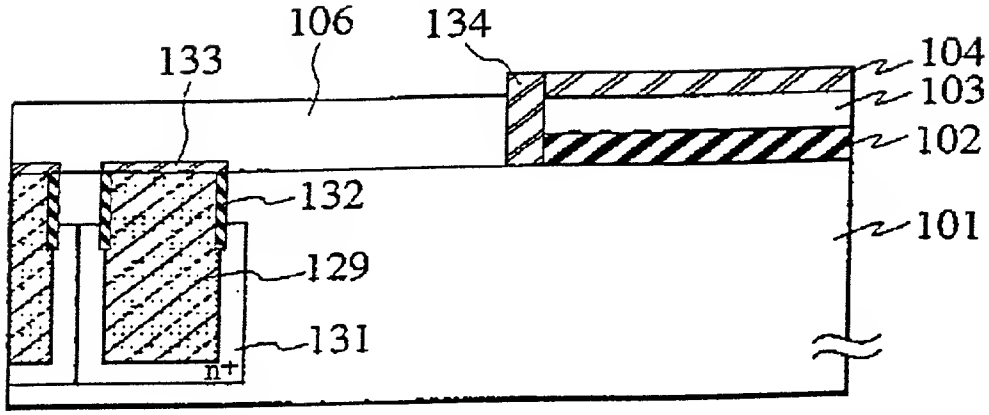

FIG.11E

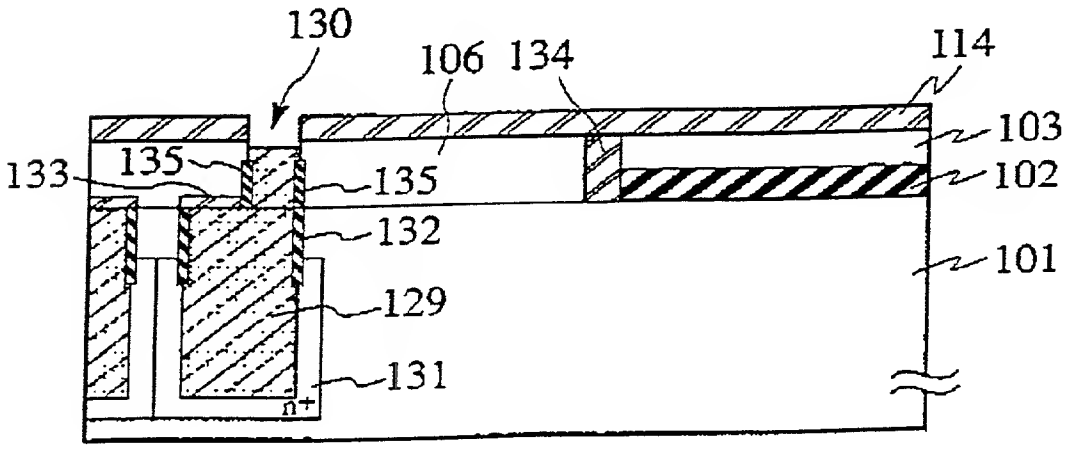

FIG.11F

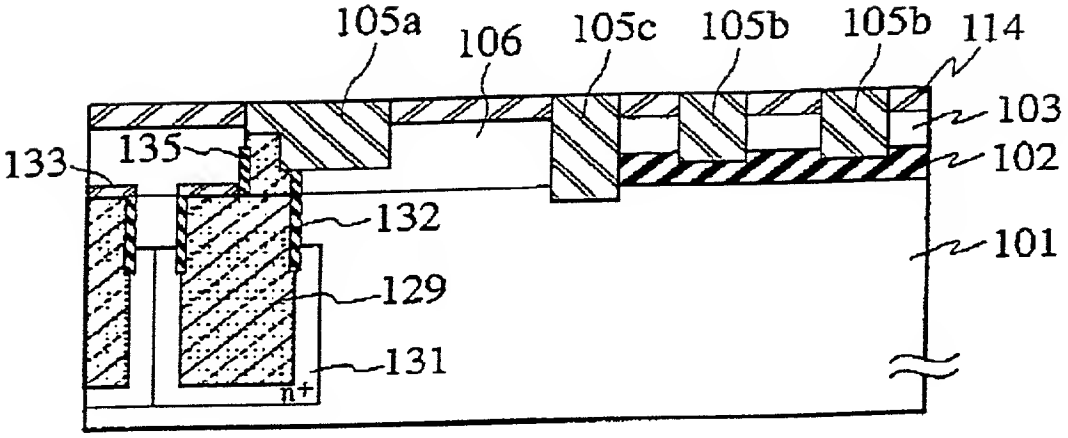

FIG.11G

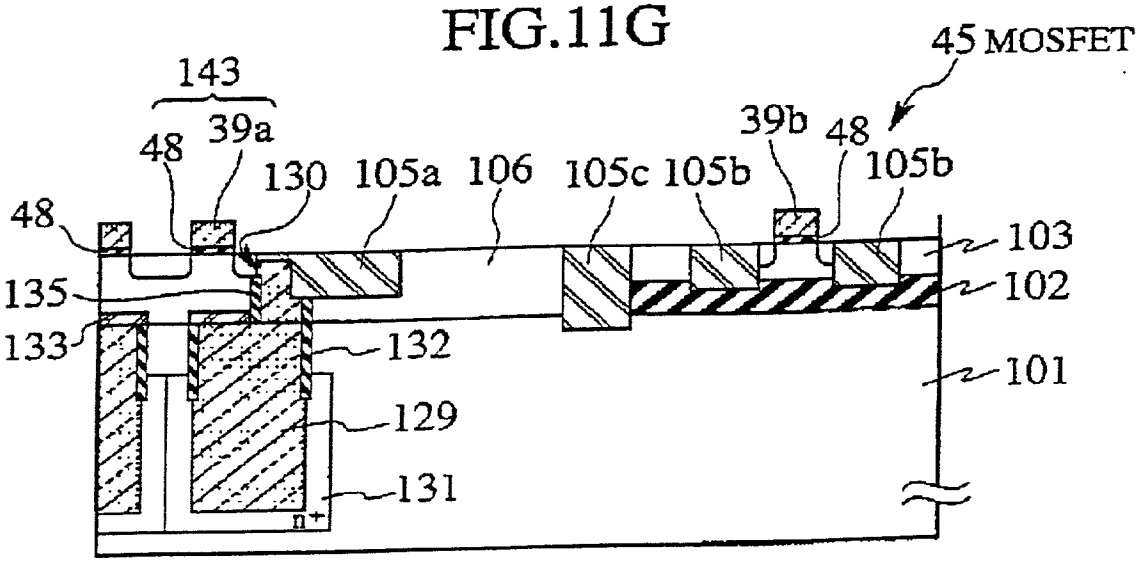

FIG.12

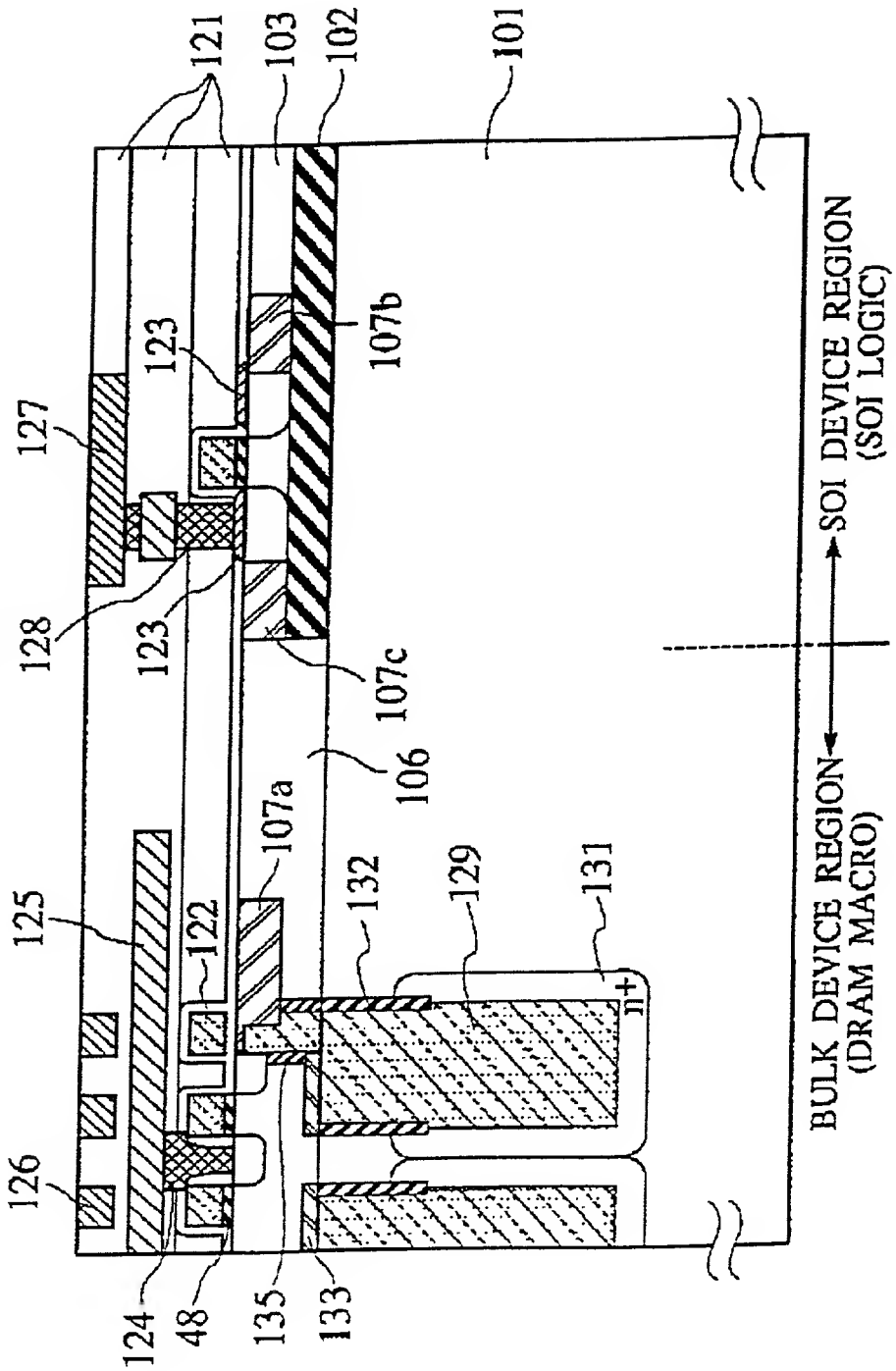
121
103
102
101
123
107b
127
128
123
107c
106
107a
125
122
132
129
131
n+
126
124
48
135
133
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.13

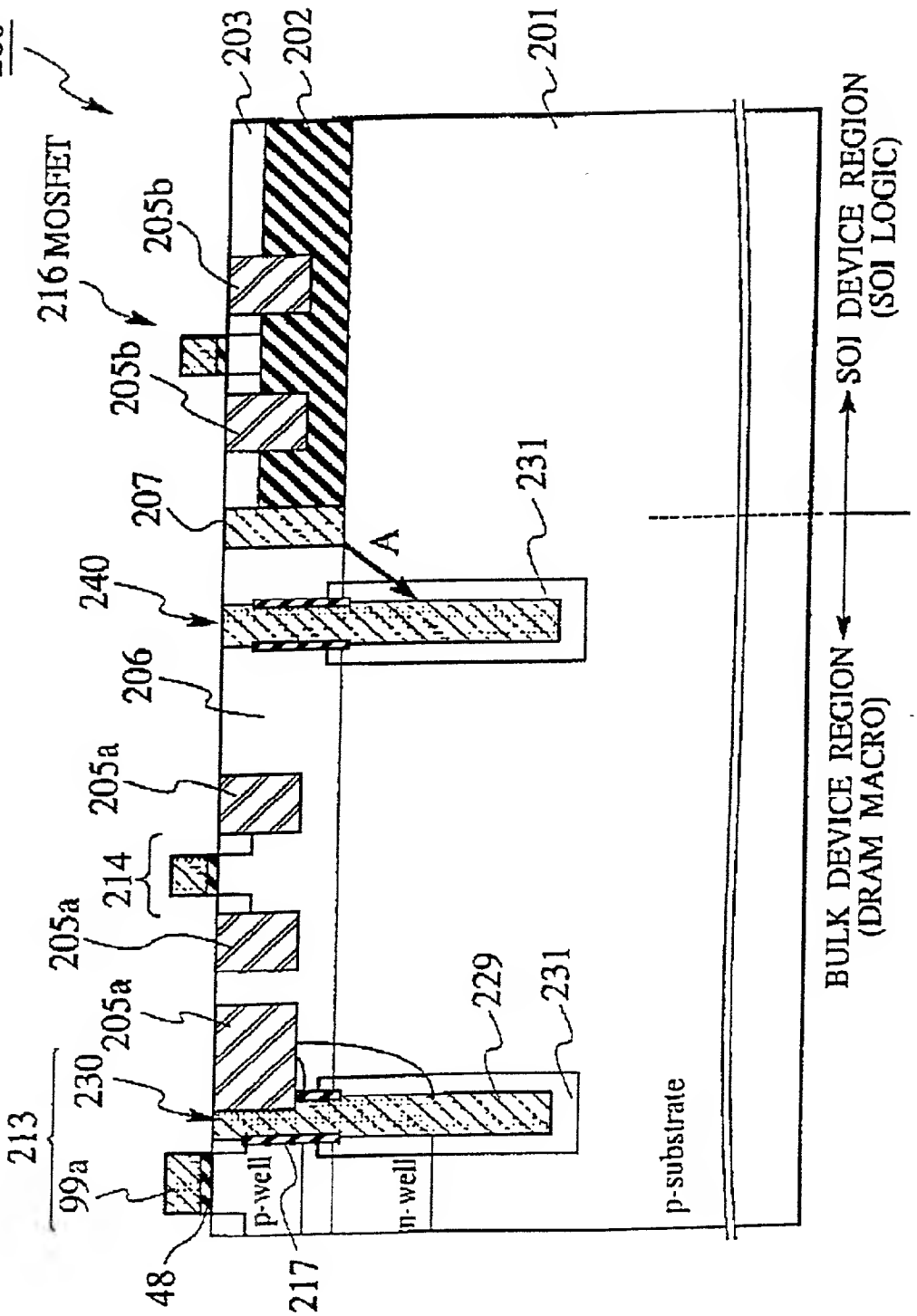
200
216 MOSFET
203
202
201
205b
205b
207
231
A
240
206
205a
214
205a
205a
230
213
99a
229
231
p-well
n-well
p-substrate
48
217
SOI DEVICE REGION
(SOI LOGIC)
BULK DEVICE REGION
(DRAM MACRO)

FIG.14

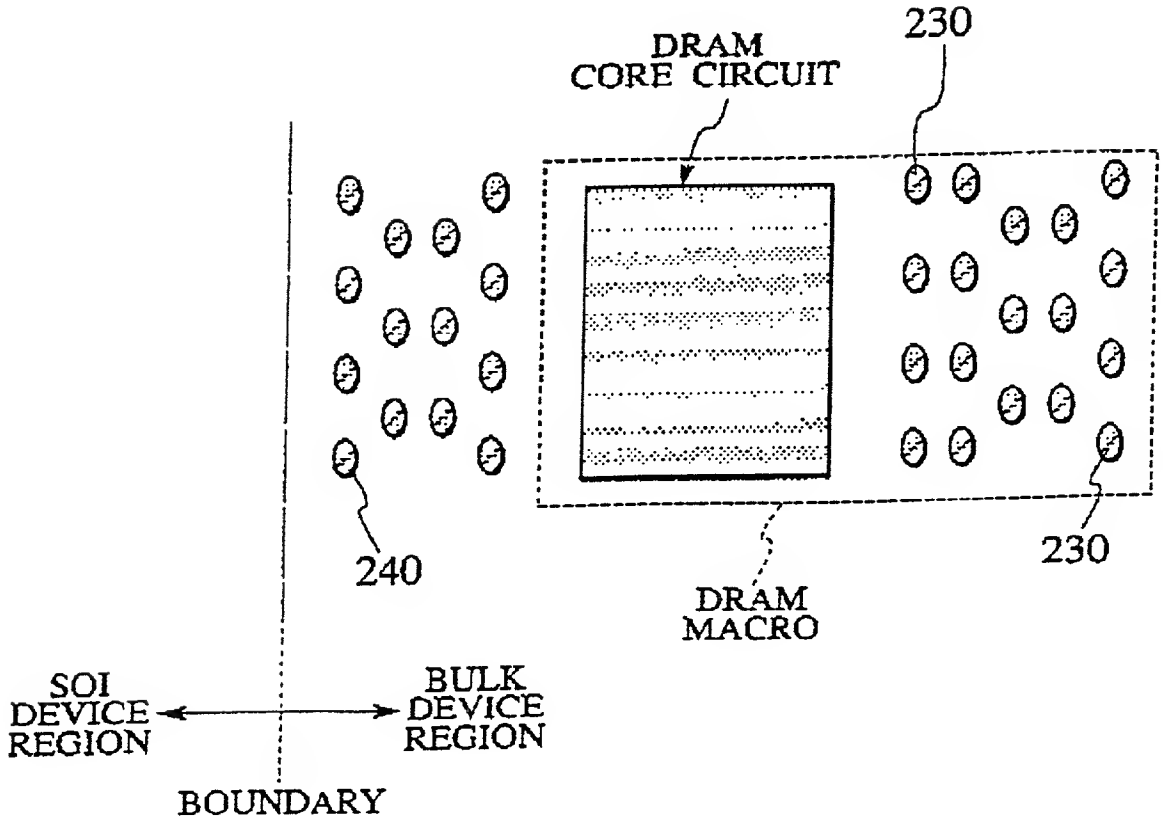
230
DRAM
CORE CIRCUIT
240
230
DRAM
MACRO
SOI
DEVICE
REGION
BULK
DEVICE
REGION
BOUNDARY

FIG.15A

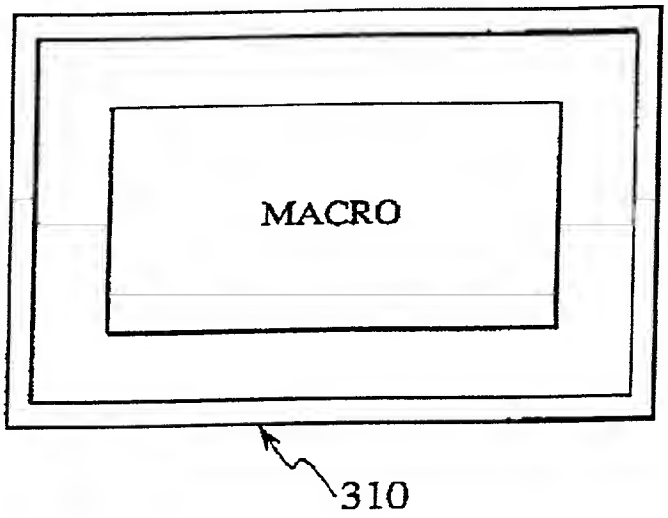
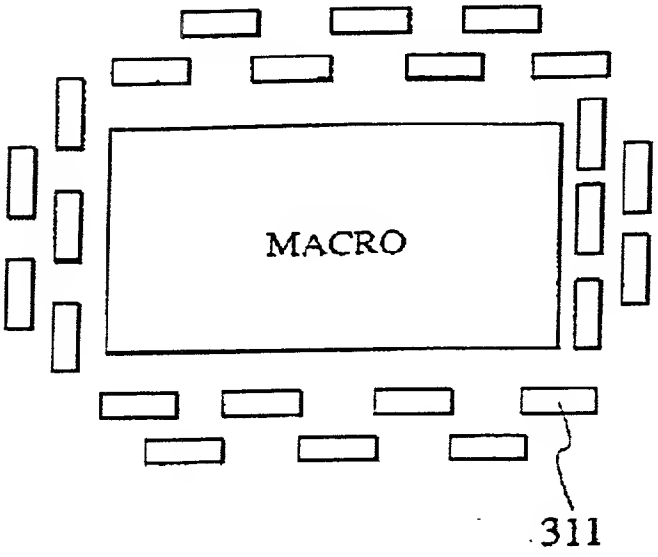
FIG.15B